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<b>(21) International Application Number:</b> PCT/US99/02959 <b>(22) International Filing Date:</b> 5 February 1999 (05.02.99)  <b>(30) Priority Data:</b> 09/019,134 5 February 1998 (05.02.98) US  <b>(71) Applicant:</b> SHENG, George, S. [US/US]; 25 Locke Street, Winchester, MA 01890 (US).  <b>(72) Inventors:</b> GONION, Jeffry, E.; 217 Lancelot, Palatine, IL 60067 (US). BILBREY, Brett, C.; 5900 Prairie Lane, Palatine, IL 60067 (US).  <b>(74) Agents:</b> PERKINS, Jefferson et al.; Foley & Lardner, Suite 3300, 330 North Wabash Avenue, Chicago, IL 60611-3608 (US).		<b>(81) Designated States:</b> JP, KR, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).  <b>Published</b> <i>Without international search report and to be republished upon receipt of that report.</i>
<b>(54) Title:</b> DIGITAL SIGNAL PROCESSOR USING A RECONFIGURABLE ARRAY OF MACROCELLS  <b>(57) Abstract</b>  A real time digital systolic processor with a core of reconfigurable interconnected macrocells which can be programmed according to function for processing high bandwidth digital data. Each macrocell contains arithmetic logic units for performing predetermined functions based on format of the input data stream from an outside source or from other macrocells. The interconnects between each macrocell are arranged so that the function of the device is predetermined according to user specific applications.		